**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in this application.

1.(Canceled)

2.(Currently Amended) The circuit of ~~claim 1~~ claim 8 wherein the oscillator comprises a plurality of N amplifiers each defining a different gain, and wherein the strobe comprises a most significant bit selected from an output of one of the amplifiers~~, and wherein N is an integer greater than one~~.

3.(Original) The circuit of claim 2 wherein each of the N timing signals are coupled to an output of an associated amplifier, and each timing signal except that coupled to a highest gain amplifier is independent of a most significant bit output from said associated amplifier.

4.(Currently Amended) The circuit of ~~claim 1~~ claim 8 wherein the fractional interpolator comprises:

a shift register having parallel inputs coupled to the N data inputs and to the strobe; and

N bit splitters each having an input coupled to a timing signal, for each outputting a first error value that depends at least in part from a most significant bit (MSB) defined by the timing signal and for outputting a second error value that depends at least in part from at least one other bit defined by the timing signal that is not the MSB.

5.(Currently Amended) The circuit of claim 4 wherein the fractional interpolator ~~filter~~ further comprises:

N sub-blocks each having an input coupled to an output of the shift register and an input coupled to an output of an error-formatter.

6.(Original) The circuit of claim 5 wherein the sub-blocks are of the type Farrow sub-blocks, linear interpolators, or polynomial interpolators.

7.(Canceled)

8.(Currently Amended) A circuit for re-sampling N data inputs comprising:

a timing error detector sub-circuit having a first input coupled to a symbol rate clock and a second input coupled to a strobe;

an oscillator having an input coupled to an output of the timing error-detector sub-circuit and N timing signal outputs for outputting N timing signals in parallel and a second output for outputting the strobe; and

at least one fractional interpolator having parallel inputs coupled to N data inputs in parallel and to the N timing signals in parallel, for outputting N data outputs in parallel, wherein N is an integer greater than one, ~~or equal to one~~

wherein the error detector sub-circuit operates to synchronize the strobe to a positive edge of the input that is coupled to the symbol rate clock and comprises:

a first state machine for generating and outputting a pulse based on the symbol rate clock;

a second and a third state machine in electrical parallel with one another, each having an input coupled to the strobe and to an output of the first state machine; and

wherein the oscillator input is coupled to an output of at least one of the second or third state machines.

9.(Original) The circuit of claim 8 wherein the error detector sub-circuit further comprises a loop filter defining a gain determined by a microprocessor, wherein the oscillator input is coupled to an output of the loop filter.

10.(Currently Amended) The circuit of ~~claim 7~~ claim 8 wherein the error detector sub-circuit synchronizes the strobe by adjusting a period between two consecutive strobes to match a period defined by the symbol rate clock.

11.(Currently Amended) The circuit of ~~claim 7~~ claim 8 wherein the error detector sub-circuit further comprises an oscillator data clock having an input coupled to the strobe, and an integrator having a first input coupled to an output of the oscillator data clock and a second input coupled to an output of the symbol rate clock, the integrator having an output coupled to an inverter, and wherein the oscillator input is coupled to an output of the inverter.

12.(Currently Amended) The circuit of ~~claim 1~~ claim 8 wherein ~~N is greater than one, and~~ the N data outputs are output at a rate at least equal to a symbol rate determined by the symbol rate clock.

13-21.(Canceled)